CLAIMS

[1] A phase locked loop circuit comprising:

an oscillation circuit oscillating with a frequency in accordance with a control signal and outputting a clock having a predetermined frequency;

a phase comparison circuit detecting a phase difference between a clock from the oscillation circuit and an input signal and outputting phase difference data;

a feedback circuit generating the control signal based on the phase difference data of the phase comparison circuit and a feedback signal and supplying the same to the oscillation circuit;

a frequency comparator comparing frequencies of the input signal and the clock of the oscillation circuit and outputting a signal in accordance with a frequency error;

an integration circuit integrating the signal in accordance with the frequency error of the frequency comparator;

a judgment circuit judging a direction of the frequency error from the integration result of the integration circuit; and

a gain adjustment circuit switching a feedback gain of the feedback signal based on the judgment result of

the judgment circuit.

[2] A phase locked loop circuit as set forth in claim 1, wherein the gain adjustment circuit switches the feedback gain of the feedback signal based on a sequential pattern of judgment results of the judgment circuit.

[3] A phase locked loop circuit as set forth in claim 1, wherein an integration constant of the integration circuit is adjustable.

[4] A phase locked loop circuit as set forth in claim 1, wherein the judgment circuit performs the judgment based on a predetermined threshold value and, when the judgment result is smaller than the threshold value, outputs a signal for suspending the output of the feedback signal to the gain adjustment circuit.

[5] A phase locked loop circuit as set forth in claim 4, wherein the judgment threshold value of the judgment circuit is adjustable.

[6] A phase locked loop circuit as set forth in claim 1, wherein the gain adjustment circuit does not output the feedback signal in an initial lock-in state and, when continuously receiving as input the same judgment result, sequentially increases the feedback gain.

[7] A phase locked loop circuit as set forth in claim 6, wherein the gain adjustment circuit once makes the feedback gain zero when receiving as input a judgment

result of detection of frequency error in a reverse direction due to erroneous detection in the middle of lock-in, then sequentially increases the feedback gain when continuously receiving as input the same judgment result.

[8] A phase locked loop circuit comprising:

an oscillation circuit oscillating with a frequency in accordance with a control signal and outputting multi-phase clocks having different phases from each other;

a phase comparison circuit detecting a phase difference between one clock among the multi-phase clocks from the oscillation circuit and an input signal and outputting phase difference data;

a feedback circuit generating the control signal based on the phase difference data of the phase comparison circuit and a feedback signal and supplying the same to the oscillation circuit;

a frequency comparator detecting frequency error between the input signal and the clock from a zero cross edge of the input signal based on a zero cross signal of the input signal and the multi-phase clocks of the oscillation circuit and outputting a signal in accordance with the frequency error;

an integration circuit integrating the signal in accordance with the frequency error of the frequency

comparator;

a judgment circuit for judging the direction of the frequency error from the integration result of the integration circuit; and

a gain adjustment circuit for switching the feedback gain of the feedback signal based on the judgment result of the judgment circuit.

[9] A phase locked loop circuit as set forth in claim 8, wherein the gain adjustment circuit switches the feedback gain of the feedback signal based on a sequential pattern of judgment results of the judgment circuit.

[10] A phase locked loop circuit as set forth in claim 8, wherein the frequency comparator fetches the zero cross signal of the input signal based on the multi-phase clocks of the oscillation circuit and observes from which phase to which phase the edge of the zero cross of the input data signal changed in synchronization with the one clock among the multi-phase clocks to thereby detect whether the frequency is high or low as the frequency error.

[11] A phase locked loop circuit as set forth in claim 10, wherein the frequency comparator suspends the output of the signal in accordance with the frequency error when the change of the edge of the zero cross is detected at a timing when it does not occur in a case of normal operation.

[12] A phase locked loop circuit as set forth in claim

8, wherein an integration constant of the integration circuit is adjustable.

[13] A phase locked loop circuit as set forth in claim 8, wherein the judgment circuit performs the judgment based on a predetermined threshold value and, when the judgment result is smaller than the threshold value, outputs a signal for suspending the output of the feedback signal to the gain adjustment circuit.

[14] A phase locked loop circuit as set forth in claim 13, wherein the judgment threshold value of the judgment circuit is adjustable.

[15] A phase locked loop circuit as set forth in claim 14, wherein the gain adjustment circuit does not output the feedback signal in an initial lock-in state and, when continuously receiving as input the same judgment result, sequentially increases the feedback gain.

[16] An information reproduction apparatus for sampling a signal read from a recording medium based on a clock to convert it to a digital signal for reproduction, comprising:

a phase locked loop circuit for making a sampling phase by the clock match with a correct state, wherein

the phase locked loop circuit has:

an oscillation circuit oscillating with a frequency in accordance with a control signal and

outputting a clock having a predetermined frequency,

a phase comparison circuit detecting a phase difference between a clock from the oscillation circuit and an input signal and outputting phase difference data,

a feedback circuit generating the control signal based on the phase difference data of the phase comparison circuit and a feedback signal and supplying the same to the oscillation circuit,

a frequency comparator comparing frequencies of the input signal and the clock of the oscillation circuit and outputting a signal in accordance with a frequency error,

an integration circuit integrating the signal in accordance with the frequency error of the frequency comparator,

a judgment circuit judging a direction of the frequency error from the integration result of the integration circuit, and

a gain adjustment circuit switching a feedback gain of the feedback signal based on the judgment result of the judgment circuit.

[17] An information reproduction apparatus as set forth in claim 16, wherein the gain adjustment circuit switches the feedback gain of the feedback signal based on a sequential pattern of judgment results of the judgment

circuit.

[18] An information reproduction apparatus as set forth in claim 16, wherein the judgment circuit performs the judgment based on a predetermined threshold value and, when the judgment result is smaller than the threshold value, outputs a signal for suspending the output of the feedback signal to the gain adjustment circuit.

[19] An information reproduction apparatus as set forth in claim 16, wherein the gain adjustment circuit does not output the feedback signal in an initial lock-in state and, when continuously receiving as input the same judgment result, sequentially increases the feedback gain.

[20] An information reproduction apparatus as set forth in claim 19, wherein the gain adjustment circuit once makes the feedback gain zero when receiving as input a judgment result of detection of frequency error in a reverse direction due to erroneous detection in the middle of lock-in, then sequentially increases the feedback gain when continuously receiving as input the same judgment result.

[21] An information reproduction circuit for sampling a sine wave state signal read from a recording medium based on clocks to convert it to a digital signal for reproduction, comprising:

a phase locked loop circuit for making a sampling

phase from the clock match with a correct state, wherein

the phase locked loop circuit has

an oscillation circuit oscillating with a frequency in accordance with a control signal and outputting multi-phase clocks having different phases from each other,

a phase comparison circuit detecting a phase difference between one clock among the multi-phase clocks from the oscillation circuit and an input signal and outputting phase difference data,

a feedback circuit generating the control signal based on the phase difference data of the phase comparison circuit and a feedback signal and supplying the same to the oscillation circuit,

a frequency comparator detecting a frequency error between the input clock and the clock from a zero cross edge of the input signal based on a zero cross signal of the input signal and the multi-phase clocks of the oscillation circuit and outputting a signal in accordance with the frequency error,

an integration circuit integrating the signal in accordance with the frequency error of the frequency comparator,

a judgment circuit judging the direction of the frequency error from the integration result of the

integration circuit, and

a gain adjustment circuit switching the feedback gain of the feedback signal based on the judgment result of the judgment circuit.

[22] An information reproduction apparatus as set forth in claim 21, wherein the gain adjustment circuit switches the feedback gain of the feedback signal based on a sequential pattern of judgment results of the judgment circuit.

[23] A phase locked loop circuit as set forth in claim 21, wherein the frequency comparator fetches the zero cross signal of the input signal based on the multi-phase clocks of the oscillation circuit and observes from which phase to which phase the edge of the zero cross of the input data signal changed in synchronization with the one clock among the multi-phase clocks to thereby detect whether the frequency is high or low as the frequency error.

[24] A phase locked loop circuit as set forth in claim 23, wherein the frequency comparator suspends the output of the signal in accordance with the frequency error when the change of the edge of the zero cross is detected at a timing when it does not occur in a case of normal operation.

[25] An information reproduction apparatus as set forth in claim 21, wherein the judgment circuit performs the judgment based on a predetermined threshold value and,

when the judgment result is smaller than the threshold value, outputs a signal for suspending the output of the feedback signal to the gain adjustment circuit.

[26] An information reproduction apparatus as set forth in claim 25, wherein the gain adjustment circuit does not output the feedback signal in an initial lock-in state and, when continuously receiving as input the same judgment result, sequentially increases the feedback gain.